

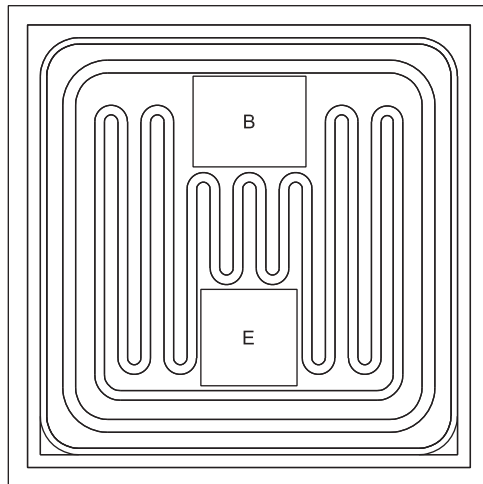
PROCESS CP710V
Small Signal Transistor
PNP - High Voltage Transistor Chip



PROCESS DETAILS

Process	EPITAXIAL PLANAR
Die Size	26 x 26 MILS
Die Thickness	7.1 MILS
Base Bonding Pad Area	6.1 x 4.9 MILS
Emitter Bonding Pad Area	5.2 x 5.2 MILS
Top Side Metalization	Al - 30,000Å
Back Side Metalization	Au - 18,000Å

GEOMETRY



GROSS DIE PER 5 INCH WAFER

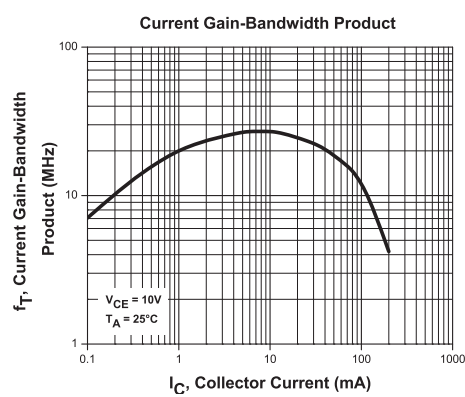
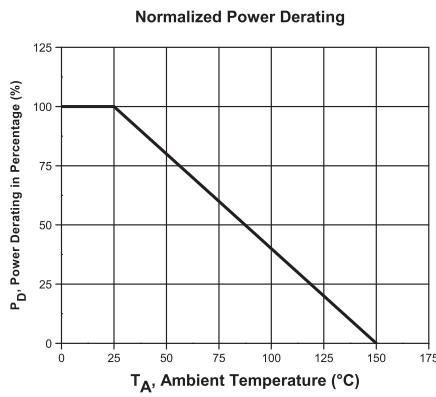
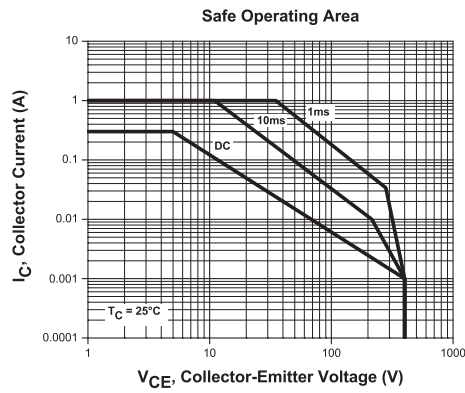
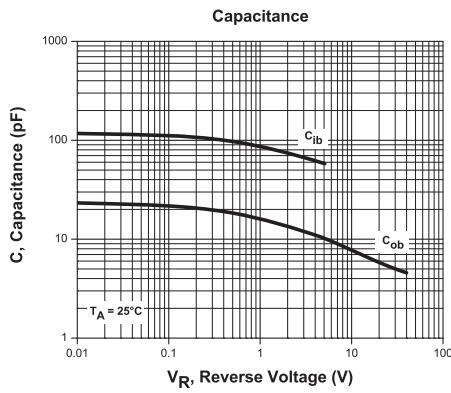
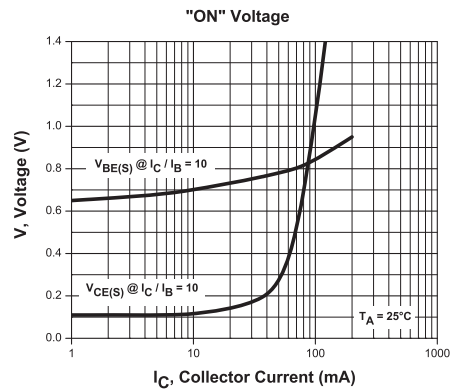
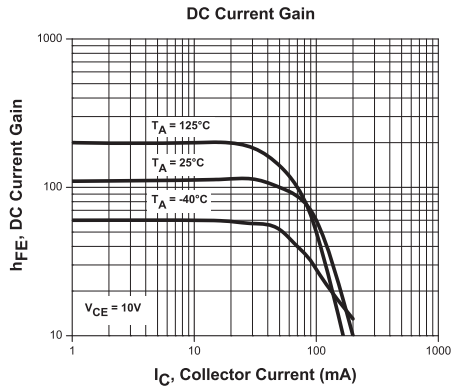
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PRINCIPAL DEVICE TYPES

CMLTA94
CMPTA94
CMPTA92E
CXTA92
CZTA92
CZTA94

PROCESS CP710V

Typical Electrical Characteristics



R0 (5-August 2010)